An Efficient Microprocessor Based Firing Scheme for Three-Phase Converter

Vibhu Jately, Puneet Joshi, Sudha Arora

Abstract- Inter-grid flow of power through D.C. link is being employed in large power systems for improving the stability. The direction of power flow being controlled by the voltage difference between the two ends of the D.C. link makes the control scheme simple. A laboratory scheme of the firing circuit of the converter used in the D.C. link is designed and built. The entire scheme consists of a ZCD (Zero crossing detector) to identify the positive going zero of the A.C. input which is then fed to 8085 microprocessor for generating the required pulses in order to fire the three phase fully controlled full wave converter. The scheme requires minimum number of electronic components since it utilizes the same circuit for rectification and inversion mode of operation.

Index Terms- distributed power system, fully controlled thyrsitor bridge, microprocessor based firing scheme

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1 INTRODUCTION

The demand for reliable energy is growing while the society depends more and more on electricity. Since the late 20th century renewable energy resources e.g. hydro, solar, wind, bio-mass, etc. have entered the market and are rapidly growing each day. Interfacing these resources to the grid has caught the interest of investigators in a big way. Avoiding outages in such interface connections is a matter of priority among engineers involved in design and operation of distributed power system. In the early days, the first distribution systems were based on DC technology but were rapidly replaced with AC systems due to ease of raising of ac voltage levels for transmission, and then again lowering these voltage levels at the load end by use of transformers.

Due to the better efficiency and good level of controllability within power electronics technologies, an LVDC system has the potential to be used in the "last mile" network (consumer end). The use of D.C. power for transmission is becoming more popular these days due to its capacity to transfer large amount of power as compared to an A.C. line. Despite the losses in the converter station, D.C. transmission is preferred over A.C. due to the absence of reactive power component. In addition, the skin effect, which is caused by eddy currents induced by the changing magnetic field of A.C. currents, increases the resistance of the A.C. line, but has no effect on the resistance of D.C. line.

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An LVDC distribution system will also facilitate the connection of renewable energy systems. An LVDC network is also suitable for the connection of large number of D.C. loads. Absence of harmonics, power factor correction and grid synchronization are some major advantages of using D.C. system over its A.C. counterpart.

The transmission of power to the grid also involves DC transmission lines due to their cost benefits. In such transfer of power various authors [1], [2] have proposed a variety of firing schemes for the operation of converters. The firing scheme proposed here is simple, built around components and microprocessor available in most laboratories, and found reliable in tests conducted in laboratory. It has though been used in low voltage applications with thyristors valves, but can easily be extended for use in HVDC applications where MCT, GTO are employed as also in DC transmission for inter grid connections of two or more AC grids.

This reliable, cheap and robust scheme has been tested and employed in both LVDC and MVDC applications for the firing of converters and also for use in inversion mode for bi-directional power flow on a dc link.

2 MATERIALS AND METHODS

The firing scheme of the three-phase converter consists of a zero crossing detector, Intel 8085 microprocessor, and an isolation circuit, that separates the firing circuitry from the higher voltage side. In a three-phase supply, all the phases are 120 electrical degrees apart. One of the phases is arbitrarily selected as a reference phase for zero crossing detection. The firing pulses for all six thyristor valves in the bridge were generated using this phase as the reference. The scheme, hence requires to maintain the 120° lag/lead among the corresponding thyristors valves of the three phases.

Establishing the positive going zero point on the reference phase was thus a primary requirement. This was done using a zero crossing detector circuit explained below.

2.1 Zero Crossing Detector

The reference phase voltage is stepped down using a 230V/6V transformer. The output of the transformer is fed to the non-inverting terminal of popular op-amp (741 IC), keeping its inverting terminal grounded. In absence of any feedback component, the op-amp works as a simple comparator driving its output terminal to saturation levels corresponding to the positive and negative supplies of the op-amp. This results in the sinusoidal 6V input fed to the non-inverting terminal being converted into a square wave. The negative half cycles of the square wave are removed by using a rectifier diode. The amplitude level of this train of positive pulses is reduced to a level that is compatible with the microprocessor and its support chips. Finally the output of the zero crossing detector (ZCD) is fed to programmable peripheral interface, a support chip of microprocessor 8085. A software explained later polls this output of this zcd to detect the positive going zero of the reference phase. The output waveform of the zcd is compared with the waveform of the reference phase using a four-channel tektronix digital storage oscilloscope. The block diagram of the circuit used to achieve zero crossing detection is shown in Fig. 1.

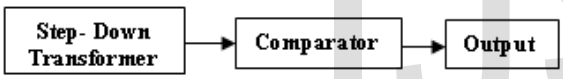

Fig. 1 Block diagram of zero crossing detector circuit

2.2 Interfacing with 8085 microprocessor

The Intel 8085 microprocessor has been used for the purpose of zero crossing detection. The ports of 8255-I are programmable, and can be configured to be used as 8-bit input or output ports. In this scheme port-B has been selected as an input port and port-A as an output port. The ports are initiated by feeding in an appropriate control word to match the configuration of port-B as input and port-A as an output port. The output of the ZCD if fed to the pin corresponding to the least significant bit of port-B, PB0 of PPI. To avoid the recording of a false data due to any spurious signals, the remaining pins PB1-PB7 of PPI have been kept grounded in the scheme. The output pulses, responsible for getting the proper firing sequence of thyristors valves, are obtained at port A (output port). These pulses at pins (PA0-PA5) of PPI 8255-I chip is further fed to the amplification/ isolation circuit.

2.3 Amplification/Isolation Circuit

The output current levels of 8255A has IOL specification of 1.7mA and IOH specification of 200µA[3]. These output current levels are not sufficient enough for gating purposes of most thyristors valves used in converters. Some amplification of these current levels becomes mandatory. In the current scheme a set of two darlington pairs, one for each phase have been used. This way six darlington pairs have been employed one for each thyristor valve. To achieve a complete isolation between the low voltage microprocessor circuit and the line voltage level of the thyristors bridge an opto-isolator has been used. A set of six opto-isolators thus isolated the controlled circuitry from the power lines. Figure 2 shows the model of the entire firing scheme.

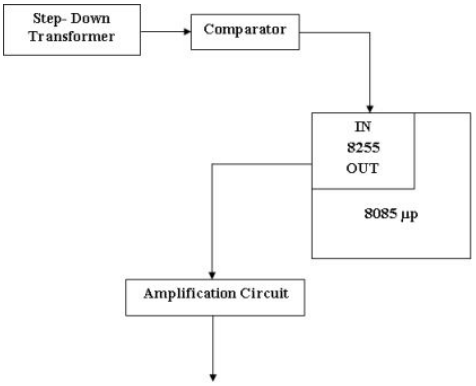

Fig. 2 The complete firing scheme model

3 Theory

The software is required to first detect the positive going zero instant on the reference phase. Then, it is required to generate control signals responsible for firing the thyristors at the desired firing angles delayed from the positive going instant of the reference phase. The developed software program continuously polls the ZCDs output that was fed to PB0. Depending upon the result of comparison of data corresponding to two successive pulses, zero and carry flags are changed and zero crossing detection is accomplished as suggested by [4] indicated in Table 1.

0 (low)	1 (high)	CF=0 ,ZF=0
0	0	CF=0 ,ZF=1
1	0	CF= 1 ,ZF=0
1	1	CF=0 , ZF=1

CF- carry flag

ZF- zero flag

Table 1- Flags

Once the instant of positive going zero is known, the software goes into a delay subroutine, which can be programmed for a change in a single location for recording the firing angle. The delay corresponding to a firing angle $\alpha=0^{\circ}$ will be 30° [5]. Here α is the firing angle from the instant of phase crossover point in a three-phase system.

The software, on return to the main program, generates the first pulse at a delay of 300 for α=0̊ at pin PA0 of PPI. As stated already, the value of α can be easily changed by a single data entry at a predefined address on microprocessor board without any change in the main program or in delay routine.

The second pulse is then generated at PA1 by calling the same subroutine but this time for 600. This is continued till all the six pulses are generated and then the pointer is sent back to the comparison loop. The algorithm described is shown in Fig. 3.

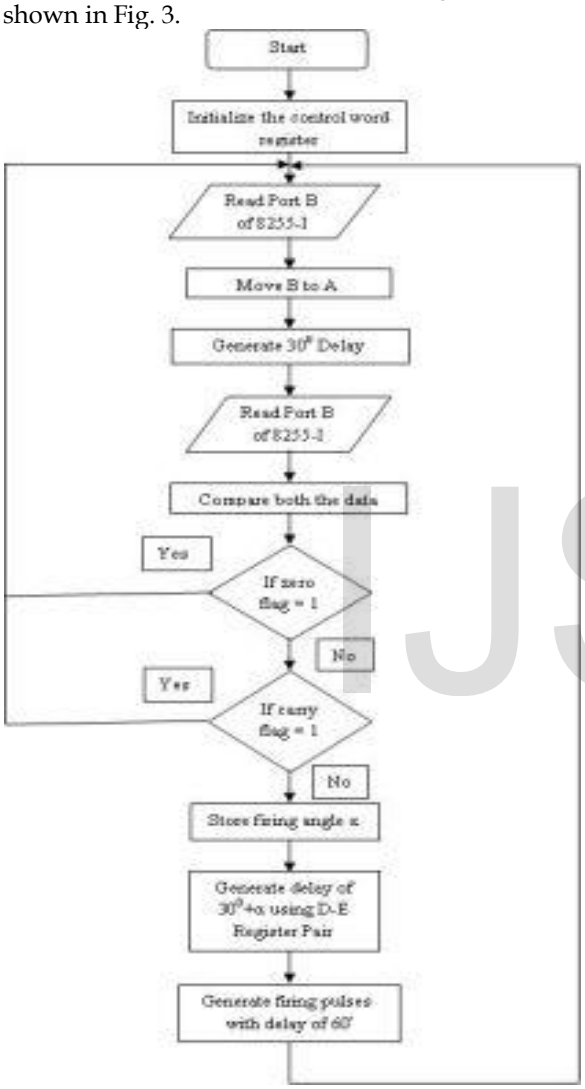

Fig. 3 Flow chart

4 Experimental Results

The firing circuit was built and tested and the experimental waveforms of Zero crossing detector, and the firing pulses for (firing angle=00) were recorded on a four-channel tektronics digital storage oscilloscope. These recorded oscillograms are shown in Figure 4 and Figure 5, respectively. The theoretical waveforms are correlated with the experimental waveforms. The operation of the scheme has been found out to be stable.

The output of the ZCD (yellow) which is the positive train of pulses is compared with the phase voltage (blue). Both the signals are in phase as shown below in a four channel oscilloscope.

The firing pulses generated at PA0-PA2 are shown in Fig.5. The pulses are compared with the phase voltage for firing angle (α) = 00.

The remaining pulses PA2-PA5 are shown below in Figure 6.

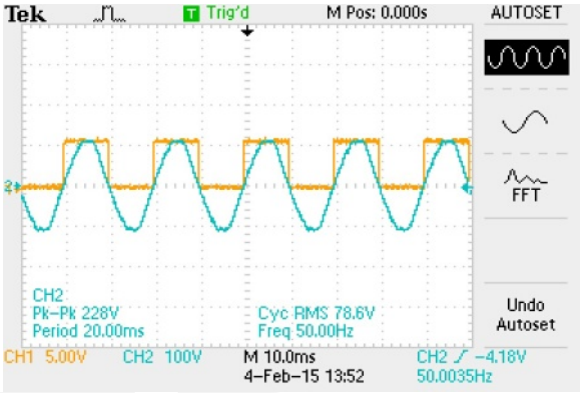

Fig. 4 Waveform of Zero Crossing Detector

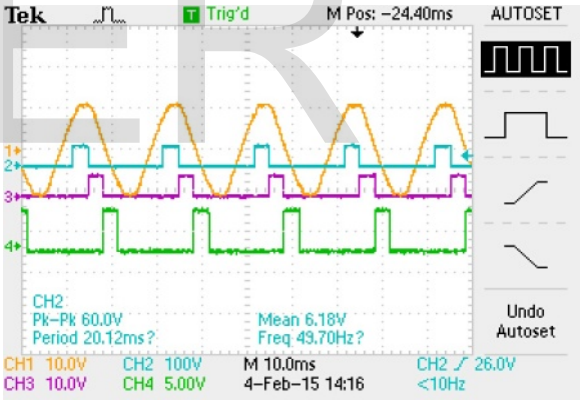

Fig. 5 Firing Pulses (PA_0-PA_2) generated from the 8085 microprocessor

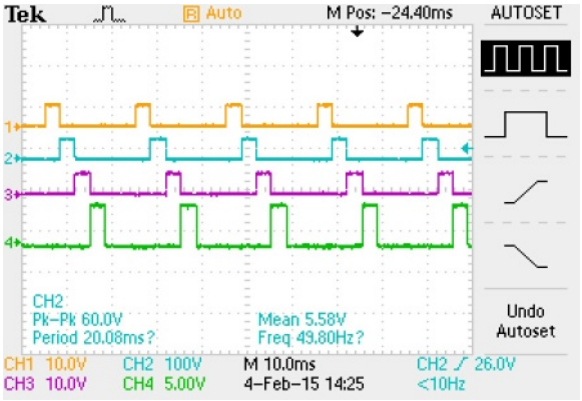

Fig. 6 Firing Pulses (PA2-PA5) generated from the 8085 microprocessor

CONCLUSIONS

A firing scheme for three-phase full wave fully controlled converter is designed and built. The scheme utilizes the same circuit for rectification and inversion modes of operation. The triggering of thyristors is achieved by using a train of pulses to make the scheme suitable for highly inductive load also. The developed scheme is being used by the authors for interfacing renewable energy resources (e.g. Photovoltaic, Wind etc.) to the grid.

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